REMARKS

Examiner Asok K. Sarkar is thanked for carefully examining and reviewing the subject patent application. The claims and the specifications have been amended in accordance with the Examiner's kind suggestions, and all claims are now believed to be in condition for allowance.

Note, in this Preliminary Amendment there are no new issues or limitations presented.

Independent claims 1 and 14, the associated dependent claims 5, 6, 9, 10, 11, 12, 13, and 26, have been amended to better define the Applicant's invention and to narrow the scope of these claims, so as to prevent interference from cited Prior Art.

BRIEF SUMMARY OF THE INVENTION

It is a general object of the present invention to provide an improved method to form a copper diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing, for 0.10 micron nodes in MOSFET and CMOS applications. The diffusion barrier is formed by first depositing a tungsten

nitride bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and then finally depositing a final top layer of tungsten. This invention is used to manufacture reliable metal interconnects and contact vias in the fabrication of MOSFET and CMOS devices for both logic and memory applications. The copper diffusion barrier formed, W/WSiN/WN, passed a stringent barrier thermal reliability test at 400 °C. For pure single barrier layers, i.e., single layer WN, these exhibited copper punch through or copper spiking during the stringent barrier thermal reliability test at 400 °C.

CLAIM REJECTIONS - 35 USC 103:

The Examiner's objections to claims 1 - 10, 12 - 23, 25 and 26 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Danek et al.(US 5,942,799, hereafter referred to as Danek), and Hsu et al.(US 6,194,310 B1, US 6,054,382, hereafter referred to as Hsu), are believed to be overcome, based on the following.

In reference to Edelstein, the main purpose and focus of Edelstein's invention is exactly as its title indicates, "COPPER INTERCONNECTION STRUCTURE INCORPORATING A METAL SEED

LAYER." The focus is on forming copper alloys and other metals as s ed layers. Most dual damascene processes for forming interconnection wiring incorporate metal diffusion barrier layers, as Edelstein's claim 25 states: "An interconnection system according to claim 24, wherein said diffusion barrier layer is deposited of a material selected from the group consisting of Ti, Ta, Nb, Mo, TaN, W, WN, TiN, TaSiN, WSiN, TiAlN and TiSiN."

Agree with Examiner that Edelstein fails to teach the method of the Applicant's invention, namely:
the formation of an improved copper metal diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing with 0.10 micron nodes for MOSFET and CMOS applications. The diffusion barrier is formed by depositing a tungsten nitride, WN, bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and depositing a final top layer of tungsten, W. It is not obvious exactly what barrier material or materials yield good adhesion and barrier properties, and enhances both copper seed deposition and copper electro-plating. In addition, it is not obvious exactly what processing conditions are optimum to achieve new and unexpected results.

In reference to Danek, the main purpose and focus of Danek's invention is to demonstrate the ease of deposition by a chemical vapor deposition, multi-station module or cluster tool. Applicant's invention teaches specifically the three component barrier layer: W/WSiN/WN, whereas Danek's invention teaches alternating layers of material (A) and material (B). In addition, Danek's invention does not contain any claims to diffusion barrier compounds, elements, layers or material. See Danek, Claims 1 through 19. Danek's Figs. 1, 2, 4 and 6 are close to the Applicant's Invention, but do have significant differences from the Applicant's limited claims to the three component barrier layer: W/WSiN/WN.

Agree with the Examiner that Danek, in the Specification Section, and not in the claims, does show in the figures some related barrier structures. Please see the Applicant's Amended Claim 1 enclosed. An effort was made to limit the scope of Applicant's Claim 1, namely, to the specific three component layering of the barrier layers, specific processes and specific thickness ranges, to avoid inteference with the Prior Art cited by the Examiner.

The applicant's invention is different from Hsu's invention, in that, the Applicant's invention saves some processing steps. The Applicant's invention teaches a deposition of WN, bottom layer, then silane soak for WSiN, followed by deposition of W, top layer. Only two deposition steps are required, instead of three.

Agree with the Examiner that Danek and Hsu fail to teach the Applicant's dual damascene process integration with a barrier layer.

Politely disagree with the Examiner, in that the Applicant's invention demonstrates diligence and reduction to practice in the processing conditions found in the depend claims. Also, there may exist similar process steps related to general semiconductor processing and dual damascene processing. There are many common elements amongst the Prior Art that the Examiner has cited.

The Examiner's objections to claims 11 and 24 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Danek et al.(US 5,942,799, hereafter referred to as

Danek), and Hsu et al.(US 6,194,310 B1, US 6,054,382, hereaft r referred to as Hsu), as applied to claims 1 and 14 above, and further in view of Yu et al.(US 6,291,332 B1) and Hsu et al.(US 6,054,382) are believed to be overcome, based on the following.

In reference to Yu, as the title of the invention states, "Electroless Plated Semiconductor Vias and Channels," Yu teaches a plating method for dual damascene. Yu's Column 2, line 28 to 40, emphasizes the need for the copper seed layer to have <111> crystal orientation, as the Applicant's invention achieves. Yu's claim 6 mentions some common barrier layer materials, with elemental W being the only material common to just one layer of the Applicant's invention.

In regards to the Examiner's objections to the Applicant's claim 11 and 24 referencing the formation of fine grained <111> plated Cu, as being obvious over Edelstein, in view of Danek and Hsu, and further in view of Yu and Hsu, are believed to be overcome, based on the following.

Agree with the Examiner that fine grain <111> for seed and plated copper is desirable, but by what methods, can one achieve a <111> copper seed layer consistently and reliably

on a dual damascene barrier layer. The Applicant's invention demonstrates the development of a process that achieves good properties in the seed and plated copper, and that has passed stringent reliability tests for copper interconnect wiring.

The Examiner's objections to claims 1 - 13 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Koyama et al.(US 5,990,008, hereafter referred to as Koyama), are believed to be overcome, based on the following.

In Koyama's invention, with reference to column 7, lines 4 - 17, "W is used as the first layer, a second layer of WSiN may be used." Acknowledge the Examiner's remarks that Koyama teaches just a dual barrier layer. This is substantially different from the Applicant's invention, which a deposition of WN, bottom layer, then silane soak, followed by deposition of W, top layer. Only two deposition steps are required, instead of three. The sequence, selection of material and processing of the Applicant's invention are critical for good adhesion properties, good <111> copper plating and good electrical properties of the inlaid plated copper interconnects.

In Addition, Koyama claims only two material layers for the barrier layer, namely Ti and TiN, please see Koyama's Claims 9,10, 19,20, 29,30, 39 and 40.

In conclusion, for state-of-the-art advanced applications in silicon technology, the Applicant's invention is believed to be patentable over these various references, because there seems to be insufficient basis for concluding that the modification of Prior Art disclosures would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination.

FINAL REMARKS

The Examiner Asok K. Sarkar is again thanked for carefully examining and reviewing the subject patent application. The specifications and claims have been reviewed in accordance with all the Examiner's kind suggestions, and after amending the specifications and claims in accordance with the Examiner's helpful suggestions, all claims are now believed to be in condition for allowance.

All rejected Claims 1 - 26 are now believed to be in allowable condition, and allowance is so requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned, "Version With Markings to Show Changes Made."

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

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Version With Markings to Show Changes Made

PLEASE AMEND THE CLAIMS AS FOLLOWS:

1. (AMENDED) A method of preventing copper diffusion in the fabrication of an integrated circuit by means of a composite diffusion barrier layer, and forming conducting inlaid copper, the method comprising the following steps:

(a) providing a substrate or wafer having an insulator layer deposited upon said substrate;

(b) providing a first level of conducting wiring over said insulator layer;

(c) depositing a first and second dielectric layer over said first level of conducting wiring;

(d) patterning and etching the dielectric layers forming dual damascene trench/via openings;

(e) depositing a WN first barrier layer over said dielectric layers covering and lining said trench/via;

(f) soaking said WN first barrier layer in a reactive silane gas mixture [to] forming a WSiN layer on the WN; [, thus forming a composite barrier layer consisting of top layer to bottom layer of WSiN/WN diffusion barrier layer.]

(g) depositing a W barrier layer over the WN first barrier layer and on the WSiN layer, forming over dual damascene trench/via openings, by the above process

steps (a) to (g), a composite diffusion barrier layer comprised of W/WSiN/WN, with a WN first barrier layer, followed by a WSiN layer on the WN first barrier layer, and then followed by a W barrier layer on the WSiN layer;

(h) depositing by electrochemical deposition a copper seed layer over the diffusion barrier layer;

(i) depositing by electrochemical deposition a copper conducting material on the copper seed layer forming an excess of copper, and removing the excess material, thus forming conducting inlaid copper.

5. (AMENDED) The method of claim 1, wherein the [top barrier layer of] W barrier layer on the WSiN layer [, when applicable,] is deposited by chemical vapor deposition (CVD) or by physical vapor deposition (PVD), sputtering, in the thickness range from about 30 to 50 Angstroms.

6. (AMENDED) The method of claim 1, wherein the trench or channel and via hole contact is lined with a diffusion barrier layer comprised of
[a composite barrier with a top layer of WSiN, thickness from about 30 to 60 Angstroms and a bottom layer of WN, thickness from about 30 to 50 Angstroms.]

a composite diffusion barrier layer comprised of W/WSiN/WN, with a WN first barrier layer thickness from about 30 to 50 Angstroms, followed by a WSiN layer on the WN first barrier layer thickness from about 30 to 60 Angstroms, and then followed by a W barrier layer thickness from about 30 to 50 Angstroms on the WSiN layer.

9. (AMENDED) The method of claim 1, wherein [in the trench or channel and the via hole contact is lined with an adhesive copper seed layer on the diffusion barrier layer,] the copper seed layer [being] is deposited by [electrochemical deposition (ECD), or by] physical vapor deposition [(PVD)] sputtering, and the seed layer material is comprised of copper metal [layer,] thickness from about 1,000 to 2,200 Angstroms [by PVD, and thickness from about 200 to 500 Angstroms by chemical vapor deposition (CVD)].

10. (AMENDED) The method of claim 1, wherein the copper conducting material on the copper seed layer [conducting material layers] for subsequent conducting interconnect lines and via contacts is comprised of the

following conducting type materials: electrochemical deposition [(ECD)] of copper, upon the copper seed layer.

11. (AMENDED) The method of claim 1, wherein the copper conducting material on the copper seed layer [the ECD copper] is electrochemically deposited in the trench/via structures with a wide process window upon said seed layer and said barrier layer, with a fine grained <111> texture.

12. (AMENDED) The method of claim 1, wherein [each level of conducting structure] the excess of copper is planarized by removing excess material, the method being selected from the group [consisting] comprised of: planarization by chemical mechanical polish (CMP), milling, ion milling, and/or etching, which leave the copper in trench/via openings, forming single and dual inlaid structures that include conducting interconnect lines and contact vias.

13. (AMENDED) The method of claim 1, wherein multilevel conducting inlaid copper [conducting structures are] is fabricated [ing] by repeating the process steps (c) through (i) described herein.

14. (AMENDED) A method of preventing copper diffusion in the fabrication of an integrated circuit by means of a composite diffusion barrier layer , and forming conducting damascene inlaid copper, the method comprising the following steps:

(a) providing a substrate or wafer having an insulator layer deposited upon said substrate;

(b) providing a first level of conducting wiring over said insulator layer;

(c) depositing a first and second dielectric layer over said first level of conducting wiring;

(d) patterning and etching the dielectric layers forming dual damascene trench/via openings;

(e) depositing a WN first barrier layer over said dielectric layers covering and lining said trench/via;

(f) soaking said WN first barrier layer in a reactive silane gas mixture forming a WSiN layer on the WN;

(g) depositing a W barrier layer over said WN first barrier layer and over said WSiN layer, forming a composite barrier layer consisting of top layer to bottom layer of W/WSiN/WN diffusion barrier layer;

(h) depositing by electrochemical deposition (ECD) a copper seed layer over said diffusion barrier layer;

(i) depositing by electrochemical deposition (ECD) copper conducting material over said copper seed layer forming an excess of copper, and removing the excess material layers to [from] form conducting damascene inlaid copper [conducting copper dual inlaid structures] ,in the fabrication of copper interconnect wiring and contact vias.

26. (AMENDED) The method of claim 14, wherein multilevel conducting structures are fabricated [ing] by repeating the process steps (c) through (i) described herein.